Bounds for the Number of DC Operating Points of Transistor Circuits

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Abstract

A transistor circuit consisting of linear positive resistors, q exponential diodes, and p Ebers-Moll modeled bipolar transistors has at most $(d+1)^d\ 2^{d(d-1)/2}$ isolated dc operating points, where $d = q + 2p$. If, instead of bipolar transistors, the circuit employs Shichman-Hodges modeled field-effect transistors, then it can have at most $2^p 3^{2p}(4p+q+1)^q 2^{q(q-1)/2}$ isolated dc operating points. Bounds are also obtained for the number of dc operating points in circuits using other transistor models.

I. Introduction

Circuits with nonlinear elements may have multiple discrete dc operating points. In contrast, circuits consisting of positive linear resistors possess either one dc operating point, or, in special cases, a continuous family of dc operating points. We consider the problem of estimating upper bounds for the number of isolated dc operating points of circuits consisting of linear positive resistors, exponential diodes, Ebers-Moll modeled [5] bipolar transistors, and insulated-gate field-effect transistors (FETs) [21], such as metal-oxide FETs (MOSFETs). (Inductors and capacitors do not play a role in establishing a circuit's dc operating point and can be removed from the circuits by being short-circuited and open-circuited, respectively.) Lee and Willson [12] showed that a circuit containing two bipolar transistors possesses at most three isolated dc operating points. It is known that for $p \geq 2$ there exist circuits with p bipolar junction transistors that have $2^p - 1$ distinct dc operating points [27]. For piecewise-linear circuits, upper bounds for the number of isolated dc operating points were given by Belevich [2] and Fosséprez et al. [6]. Belevich considers only reciprocal circuits consisting of ideal diodes, linear positive resistors, and ideal transformers. For piecewise linear circuits consisting of linear positive resistors and p transistors modeled employing $2p$ ideal diodes, Fosséprez et al. obtained an upper bound of 2^{2p} isolated dc operating points. However, it appears that no upper bounds of any kind are known for general circuits having $p > 2$ transistors.

A circuit's operating points are solutions of a system of nonlinear equations

$$\mathbf{F}(\mathbf{x}) = \mathbf{0}. \tag{1}$$

We present explicit upper bounds for the number of isolated zeros of such systems when the circuit equations are of Sandberg-Willson form [20], under suitable assumptions on the $v - i$ characteristics of nonlinear diodes. By applying Theorem 1 given in Section III to a system of circuit equations with q exponential diodes and p Ebers-Moll modeled

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transistors, we obtain the upper bound $(d+1)^d\ 2^{d(d-1)/2}$, where $d = q+2p$. If, instead of bipolar transistors, the circuit employs Shichman-Hodges modeled field-effect transistors, the number of isolated dc operating points that the transistor circuit may have is at most $2^p 3^{2p}(4p+q+1)^q 2^{q(q-1)/2}$. These bounds on the number of dc operating points of transistor circuits are a direct application of a result of Khovanskii [10] in real algebraic geometry. We also obtain upper bounds for circuits with transistors modeled by piecewise-linear diodes and by piecewise-exponential diodes.

We note that to obtain finite upper bounds on dc operating points, it is necessary to make assumptions on the $v-i$ characteristics of nonlinear diodes used in the circuits, because there are examples of circuits having infinitely many isolated dc operating points, due to Nishi [15]. The bounds we obtain are, however, probably far from best possible for the circuits to which they apply. For circuits containing p transistors and an arbitrary number of linear positive resistors and independent current and voltage sources, it seems reasonable to conjecture an upper bound of 2^p-1 dc operating points.

II. Circuit Equations

II-A. Bipolar-Junction Transistors

We study equations for a circuit shown in Fig. 1 with q exponential diodes and p bipolar transistors given in the general Sandberg-Willson form [20], [22], [24], [25]. This is a system of $d = q+2p$ equations

$$\mathbf{QT}\mathcal{F}(\mathbf{x}) + \mathbf{Px} + \mathbf{c} = \mathbf{0}, \tag{2}$$

where

$$\mathcal{F}(\mathbf{x}) := \begin{bmatrix} f_1(x_1) \\ \vdots \\ f_d(x_d) \end{bmatrix} \tag{3}$$

and the $f_i(x_i)$ are monotone increasing functions with $f_i(0)=0$, characterizing exponential diodes. The exponential diodes have characteristics

$$f_i(x_i) = m_i(e^{n_i x_i} - 1). \tag{4}$$

The $d \times d$ constant matrices $\mathbf{P}$, $\mathbf{Q}$, and $\mathbf{T}$ possess the following properties:

(i) The $d \times d$ matrices $(\mathbf{Q},\mathbf{P})$ form a *passive pair.* That is,

$$\text{for}\quad \mathbf{x},\mathbf{y} \in \mathbb{R}^d, \quad \text{if}\quad \mathbf{Qx} = \mathbf{Py}, \qquad \text{then}\quad \langle \mathbf{x},\mathbf{y}\rangle \ge 0, \tag{5}$$

where $\langle \mathbf{x},\mathbf{y}\rangle = \sum_{i=1}^d x_i y_i$.

(ii) $\mathbf{T}$ is a block-diagonal matrix whose first p blocks are 2×2 block matrices of the form

$$\begin{bmatrix} 1 & -\alpha_{i+1} \\ -\alpha_i & 1 \end{bmatrix}, \quad 1 \le i \le p, \quad i \text{ odd}, \tag{6}$$

followed by q 1×1 blocks, each equal to 1. The controlled-source current-gains satisfy $0 \le \alpha_i, \alpha_{i+1} < 1$.

The Ebers-Moll model [5], [23] for a bipolar junction transistor consists of two nonlinear exponential diodes described by (4) in which $m_i n_i > 0$ and $m_i > 0$ for a *pnp* transistor, and $m_i < 0$ for an *npn* transistor. The 2×2 blocks in $\mathbf{T}$ that appear in $\mathbf{T}\mathcal{F}(\mathbf{x})$ in (2) model a bipolar junction transistor as a pair of linearly coupled exponential diodes.

The model parameters m_i, n_i for $1 \le i \le 2p$ also satisfy the passivity, no-gain, and reciprocity conditions given below.

An Ebers-Moll modeled bipolar transistor is *passive* [8] if and only if $f_i(x_i)$, $f_{i+1}(x_{i+1})$, and transistor current-gains α_i and α_{i+1} satisfy

$$\alpha_{i+1} \le \frac{m_i}{m_{i+1}} \le \frac{1}{\alpha_i}$$

$$\alpha_{i+1} \le \frac{n_i}{n_{i+1}} \le \frac{1}{\alpha_i}. \tag{7}$$

The assumption of the no-gain property, i.e., no temperature difference between the two transistor pn junctions, implies a common functional form (4) for $f_i(x_i)$ and $f_{i+1}(x_{i+1})$. The necessary and sufficient conditions for an Ebers-Moll model bipolar transistor to possess the *no-gain* property [26] are:

$$\alpha_{i+1} \le \frac{m_i}{m_{i+1}} \le \frac{1}{\alpha_i}$$

$$n_i = n_{i+1}. \tag{8}$$

The Ebers-Moll model parameters also satisfy the *reciprocity* condition [5]

$$m_i \alpha_i = m_{i+1} \alpha_{i+1}. \tag{9}$$

II-B. Field-Effect Transistors

We also consider circuits shown in Fig. 2 consisting of insulated-gate FET devices. We use the Shichman-Hodges transistor model [21] (called Level 1 MOSFET model in Spice [23]).

We can write equations for circuits consisting of FET devices in the form similar to the form for circuits consisting of bipolar transistors. Such circuits can be viewed as a purely resistive multi-port to which each FET device is connected via two two-ports sharing a common terminal. We let the source of each FET be the common terminal for the two-ports. (This choice lowers the upper bound on the number of operating points that we are able to obtain.) Then, the port currents i_{2k-1} and i_{2k}, are the gate and the drain-source transistor currents of the k-th FET device, respectively. The voltages x_{2k-1} and x_{2k}, are the gate-source and drain-source voltages, respectively. In the case of insulated-gate FET devices, the gate current is always zero, i.e., $i_{2k-1} \equiv 0$.

The general form of the nonlinear equations for a circuits consisting of q exponential diodes and p FET devices is a system of $d = q + 2p$ equations:

$$\mathbf{Q}\mathcal{F}(\mathbf{x}) + \mathbf{P}\mathbf{x} + \mathbf{c} = \mathbf{0}, \tag{10}$$

where

$$\mathcal{F}(\mathbf{x}) := \begin{bmatrix} 0 \\ f_2(x_1, x_2) \\ 0 \\ f_4(x_3, x_4) \\ \vdots \\ 0 \\ f_{2p}(x_{2p-1}, x_{2p}) \\ f_{2p+1}(x_{2p+1}) \\ \vdots \\ f_d(x_d) \end{bmatrix}. \tag{11}$$

Functions $f_{2k}(x_{2k-1}, x_{2k})$, for $k \leq p$, are monotone increasing functions that describe the dependence of the FET drain-source current on the gate-to-source and drain-to-source voltages in three regions of operation (cutoff, saturation, and linear, respectively). In the case of an n-channel FET, the forward region (normal mode of operation) ($x_{2k} \geq 0$) is given by relations:

$$f_{2k}(x_{2k-1}, x_{2k}) = \begin{cases} 0 & \text{if } x_{2k-1} \leq v_{th} \\ \frac{K_p W}{2L_{eff}}(x_{2k-1} - v_{th})^2(1 + \lambda x_{2k}) & \text{if } 0 < x_{2k-1} - v_{th} \leq x_{2k} \\ \frac{K_p W}{2L_{eff}} x_{2k}(2(x_{2k-1} - v_{th}) - x_{2k})(1 + \lambda x_{2k}) & \text{if } 0 < x_{2k} < x_{2k-1} - v_{th} \end{cases}, \tag{12}$$

where x_{2k-1} and x_{2k} are the gate-to-source and drain-to-source voltages, respectively; K_p is the transconductance factor, v_{th} is the threshold voltage, W and L are the channel width and length, respectively, $L_{eff} = L - 2L_D$ is the effective channel length, L_D is the lateral diffusion correcting factor, and λ is output conductance factor. The reverse region (inverted mode of operation) is characterized by similar relations obtained by inverting the signs of $f_{2k}(x_{2k-1}, x_{2k})$ and of x_{2k}, and by replacing voltages x_{2k-1} with $x_{2k-1} - x_{2k}$. Hence, each FET device is described by two sets of relations, depending whether the device operates in the forward or in the reverse mode of operation. Functions $f_k(x_k)$, $k = 2p+1, ..., d$ are monotone increasing functions with $f_k(0) = 0$, characterizing exponential diodes (4). Therefore, the degree of the polynomials $f_k(x_{k-1}, x_k)$ is at most three. FET devices also possess the passivity and the no-gain properties.

III. Upper Bounds

We consider systems of nonlinear equations of the form

$$\mathbf{A}\mathcal{F}(\mathbf{x}) + \mathbf{B}\mathbf{x} + \mathbf{c} = \mathbf{0}, \tag{13}$$

where $\mathbf{x} = (x_1,\ x_2,\ \ldots,\ x_d)$ and

$$\mathcal{F}(\mathbf{x}) := \begin{bmatrix} f_1(x_1) \\ \vdots \\ f_d(x_d) \end{bmatrix}. \tag{14}$$

This equation is equivalent to (2) with constant matrices $\mathbf{A} = \mathbf{QT}$ and $\mathbf{B} = \mathbf{P}$.

We discuss three different types of functional forms for the nonlinear diodes $f_i(x_i)$: exponential functions, piecewise-linear, and piecewise-exponential functions. The simplest model for a bipolar transistor is the Ebers-Moll model, which uses the exponential form. Piecewise-linear functions have often been used to approximate nonlinear resistors ([4], p. 76).

For exponential functions we obtain an upper bound using the following result of Khovanskii [10], [11, p. 12].

Theorem 1. (Khovanskii) *Consider a system of n polynomial equations*

$$P_i(x_1, \dots, x_n, y_1, \dots, y_d) = 0, \quad 1 \le i \le n, \tag{15}$$

in $n+d$ variables $x_1, \dots, x_n, y_1, \dots, y_d$, in which each P_i is of total degree d_i. Suppose in addition that

$$y_i = \exp\left(\sum_{j=1}^{n} n_{ij} x_j\right), \quad 1 \le i \le d, \tag{16}$$

in which all coefficients n_{ij} are real. The number of isolated real zeros in $\mathbb{R}^{n+d}$ of this system is at most

$$d_1 d_2 \cdots d_n \left(\sum_{i=1}^{n} d_i + 1\right)^d \; 2^{d(d-1)/2}. \tag{17}$$

Proof. See [11], p. 12 and Chapters 2 and 3. $\square$

The bound (17) obtained by the method of Khovanskii may not be the right order of magnitude in its dependence on d. Perhaps the right order of magnitude would replace the term $2^{d(d-1)/2}$ with c^d for some positive constant c.

Theorem 1 immediately yields the following upper bound:

Theorem 2. *Consider a system of nonlinear equations*

$$\mathbf{A}\mathcal{F}(\mathbf{x}) + \mathbf{B}\mathbf{x} + \mathbf{c} = \mathbf{0} \tag{18}$$

where $\mathbf{x} = (x_1, x_2, \dots, x_d)$ and

$$\mathcal{F}(\mathbf{x}) := \begin{bmatrix} f_1(\mathbf{x}) \\ \vdots \\ f_d(\mathbf{x}) \end{bmatrix} \tag{19}$$

has entries $f_i(\mathbf{x}) = \exp(\sum_{j=1}^{d} n_{ij} x_j)$ for $1 \le i \le d$. This system has at most

$$(d+1)^d \; 2^{d(d-1)/2} \tag{20}$$

isolated zeros.

Proof. This follows by applying Theorem 1 with $n = d$ and $d_i = 1$, for $1 \le i \le d$. $\square$

Theorem 2 applies to circuit equations with Ebers-Moll modeled bipolar transistors and exponential diodes. This is achieved by absorbing the constant terms in the nonlinear diodes (4) in the Ebers-Moll model into the constant term $\mathbf{c}$ in (18).

Theorem 2 also applies to circuit equations with Gummel-Poon transistor models [7], [9]. In the Gummel-Poon model additional functional dependence of the emitter and collector currents on the "base charge" is introduced. This dependence manifests itself in the transistor currents now being sums of exponential functions with three distinct exponents.

It may well be that a stronger upper bound than (20) is valid for system (18) of the special form

$$f_i(\mathbf{x}) = \exp(n_i x_i) \quad 1 \leq i \leq d. \tag{21}$$

For $d = 2$, the upper bound given by Theorem 2 is 18 real solutions. However, it can be shown that for $d = 2$ there can be at most 6 real solutions, as pointed out by Poonen [18]. A recent result of Nishi [17] asserts that there can be at most 5 real solutions. There are simple examples of this type having 4 real zeros. For example, the "decoupled" pair of equations

$$\begin{aligned} e^{x_1} - 2x_1 - 1 &= 0 \\ e^{x_2} - 3x_2 - 1 &= 0 \end{aligned} \tag{22}$$

has 4 real solutions.

We next consider piecewise-linear circuits, e.g., circuits with piecewise-linear modeled bipolar transistors and FET transistors [4]. In the piecewise-linear case there is very simple and well known upper bound for the number of solutions, given by Chua [3], which states that the number of isolated zeros of a system of d nonlinear equations where each function $f_i(x_i)$ is continuous piecewise-linear with k_i pieces, is

$$k_1 k_2 \cdots k_d. \tag{23}$$

This result applies with no assumption of monotonicity (or even continuity) of the diode characteristics, nor does it require that $f(0) = 0$.

Better upper bounds than (23) can sometimes be obtained for piecewise-linear circuits by taking advantage of special properties of the circuit equations, as done by Fosséprez et al. [6], Theorem 4.1. That paper also presents various examples of piecewise linear circuits that have continuous families of non-isolated zeros (ill-posed systems) (see their Examples 2.11).

We now obtain bounds for dc operating points of circuits with piecewise-exponential modeled bipolar transistors. Such models arise when approximating exponential functions in the Gummel-Poon model [9] over certain ranges of voltages where some exponential terms become negligible.

By a *piecewise-exponential function*, we mean a function $f(y)$ of the form

$$f(y) = c_{1,\ell} \exp(n_\ell y) + c_{2,\ell} y + c_{3,\ell}, \quad y_\ell \leq y < y_{\ell+1}, \tag{24}$$

where $-\infty = y_1 < y_2 < \ldots < y_{k+1} = +\infty$.

Theorem 3. *Consider a system of nonlinear equations*

$$\mathbf{A}\mathcal{F}(\mathbf{x}) + \mathbf{B}\mathbf{x} + \mathbf{c} = \mathbf{0}, \tag{25}$$

where $\mathbf{x} = (x_1, \ldots, x_d)$ *and*

$$\mathcal{F}(\mathbf{x}) := \begin{bmatrix} f_1(x_1) \\ \vdots \\ f_d(x_d) \end{bmatrix} \tag{26}$$

has entries $f_i(x_i)$ that are piecewise-exponential functions with k_i pieces of form

$$c_{1,\ell} \exp(n_\ell x) + c_{2,\ell} x + c_{3,\ell}, \quad \textit{for} \quad 1 \leq \ell \leq d. \tag{27}$$

This system has at most

$$k_1 k_2 \ldots k_d (d+1)^d 2^{d(d-1)/2} \tag{28}$$

isolated zeros.

Proof.

The set of isolated zeros of the system (26) is contained in the union of the set of isolated zeros of the $k_1 k_2 \ldots k_d$ systems of the same form that are obtained by replacing each of the f_i with one of its pieces extended to the whole range $\mathbb{R}$ of x_i, in every possible way. There are $\Pi_{\ell=1}^{d} k_\ell$ possible segment sets and each segment set contributes at most $(d+1)^d 2^{d(d-1)/2}$ zeros by Theorem 1. □

A similar extension of these results applies to FET devices modeled using piecewise-cubic functions:

Theorem 4. *Consider a system of nonlinear equations*

$$\mathbf{A}\mathcal{F}(\mathbf{x}) + \mathbf{B}\mathbf{x} + \mathbf{c} = \mathbf{0} \tag{29}$$

where $\mathbf{x} = (x_1, x_2, \ldots, x_d)$ with $d = 2p + q$ and

$$\mathcal{F}(\mathbf{x}) := \begin{bmatrix} 0 \\ f_2(\mathbf{x}) \\ 0 \\ f_4(\mathbf{x}) \\ \vdots \\ 0 \\ f_{2p}(\mathbf{x}) \\ f_{2p+1}(\mathbf{x}) \\ \vdots \\ f_d(\mathbf{x}) \end{bmatrix} \tag{30}$$

has entries $f_i(x)$ for i even, $1 \leq i < 2p$, is a piecewise cubic polynomial in variables $x_1, \ldots, x_{2p}$ with k_i pieces, and $f_i(\mathbf{x}) = 0$ for i odd, $1 \leq i < 2p$, and $f_i(\mathbf{x}) = \exp(\sum_{j=2p+1}^{d} n_{ij} x_j)$ for $2p + 1 \leq i \leq d$. This system has at most

$$3^p (4p + q + 1)^q 2^{q(q-1)/2} k_2 k_4 \ldots k_{2p} \tag{31}$$

isolated zeros.

Proof. Half of the first $2p$ equations in (29) are of degree three, and half are of degree one. The result follows by applying Theorem 1 with $n = 2p + q$, $d = q$, and $d_i = 3$ for i even and $i \leq 2p$, $d_i = 1$ for i odd and $i < 2p$, and $d_i = 1$ for $2p < i \leq d$, to obtain an upper bound for isolated zeros involving a given choice of cubic polynomial piece for each of the f_{2i}. Since there are at most $k_2 k_4 ... k_{2p}$ such choices, (31) follows. $\square$.

For circuits using FET devices modeled using (12), each f_1 has three pieces and two forms (depending on the mode of operation: normal or inverted) and the upper bound is

$$2^p 3^{2p} (4p + q + 1)^q 2^{q(q-1)/2}. \tag{32}$$

If the circuit contains no exponential diodes, its equations (29) become piecewise cubic polynomials, and $2^p 3^{2p}$ is then an upper bound for the number of isolated dc operating points.

It is interesting to note empirically that the presence of diodes in practical circuit designs does not seem to affect the number of dc operating points that the circuit possesses. Nevertheless, the diodes, being exponential nonlinearities, contribute to the upper bounds in the theorems above.[1]

Our results can be also applied to metal-semiconductor FET devices (MESFETs). Their model is similar to the model of MOSFET devices with the nonlinearities being polynomials of degree 5 [23]. The upper bound on the number of dc operating points in circuits employing MESFETs is easily obtained by applying the same approach as in Theorem 4.

Another type of FET devices are junction field-effect transistors (JFETs) [1]. The JFET dc model includes two exponential diodes that form a dc path from the gate to the drain and to the source, respectively. Our results can be extended to such devices by taking into account the two additional exponential diodes per each JFET.

IV. Concluding Remarks

The upper bounds stated in Section III depend on the particular functional form assumed for the nonlinear functions $f_i(\mathbf{x})$. This seems to be unavoidable. The function $f(x) = 2x + sin\ x$ represents a monotone increasing nonlinear diode with $f(0) = 0$, but the equation

$$f(x) - 2x - \frac{1}{4} = 0, \tag{33}$$

with the monotone increasing function $f(x) = 2x + \sin\ x$, has infinitely many real solutions. Allowing small perturbations around a "nice" function does not eliminate such examples. For example, for any $\epsilon > 0$ the system

$$f(x) - 2x - \epsilon/4 = 0, \tag{34}$$

[1] If we considered a gate of an FET transistor to be the common terminal of the two-ports by which each FET transistor is connected to the resistive multi-port shown in Fig. 2 (as one would most likely attempt because the gate of an FET would then correspond to the base of a BJT transistor) we obtain, instead, a higher upper bound of

$$2^p 3^{4p} (6p + q + 1)^q 2^{q(q-1)/2}.$$

with $f(x) = 2x + \epsilon \sin x$, has infinitely many real solutions. Note that the function $sin\ x$ is a sum of two exponentials with imaginary exponents. This shows that assumption of exponentials with real exponents in Theorem 1 is necessary for the finiteness of the upper bound. Nishi [15] recently reported that transistor circuits may possess infinitely many solutions in some cases where the diode characteristics have positive first and second derivatives, i.e., are increasing convex functions.

It would be desirable to obtain upper bounds for the number of dc operating points that were insensitive to small perturbations in the $v - i$ characteristics of elements in the circuit, because physical devices will contain such imperfections. It seems reasonable to allow only perturbations that preserve the sign of the first two derivatives. However, in view of the Nishi example [15], one still must put additional conditions on the matrices $\mathbf{A}, \mathbf{B}$ and the vector $\mathbf{c}$ in (13) to rule out infinitely many solutions. Such conditions surely exist, for if $\mathbf{A} = \mathbf{I}$ and $\mathbf{B}$ is a P_0-matrix, then it is well known that the system (13) has at most one solution for each fixed $\mathbf{c}$ whenever the $f_i(x_i)$ are monotone increasing functions, see Willson ([25], Theorem 12). It may well be that a finite upper bound can be obtained with the conditions $\mathbf{A}, \mathbf{B}$ weakened further, perhaps to the conditions on $\mathbf{QT}$ and $\mathbf{P}$ given in the Sandberg-Willson form (2).

The upper bounds of Section III do not make use of all properties that circuit equations possess. In particular, they make no use of properties (i) and (ii) of the Sandberg-Willson form equations (2), nor do they employ the passivity (7), the no-gain (8), and the reciprocity (9) properties of transistors. Improved upper bounds may be possible for such circuit equations with exponential-type diodes, assuming these properties hold. For example, it is known that the circuit equations in Sandberg-Willson form (2) for a circuit having at most two transistors ($d = 4,\ p = 2,\ q = 0$) have at most three isolated real zeros, see Lee and Willson [12]. However, one can find equations of the form of Theorem 1 for $d = 4$ that have 16 isolated real zeros.

We conclude with a brief discussion of two other methods that have been proposed to obtain upper bounds on the number of dc operating points of transistor circuits.

Nishi and Kawane [13], [14] present an interesting alternate approach to obtaining upper bounds for the number of solutions of circuit equations for nonlinear resistive circuit by assuming that the circuit elements satisfy monotone sign conditions on derivatives such as $\frac{df_i(x)}{dx} > 0$, or a convexity condition like $\frac{d^2 f_i(x)}{dx^2} > 0$, together with restrictions on the form of the matrices $\mathbf{QT}$ and $\mathbf{P}$ in (2). They announce an upper bound of 2^d operating points for systems (13) under such extra hypotheses. These papers do not provide complete details of the proof. It does seem that this general approach should yield bounds under appropriate hypotheses [16].

Another approach to obtaining upper bounds for the number of dc operating points of transistor circuits was recently outlined by Sarmiento-Reyes [19]. That paper announces a result (Theorem 1) stating an upper bound of 3^f for the number of dc operating points of a circuit consisting of bipolar transistors, positive linear resistors, and independent sources, where f is the number of "negative submatrices" appearing in certain decompositions of the circuit equations. A priori the number f of such submatrices is upper bounded[2] by

[2]For this bound see footnote 1 on page 103 of [19], where $n = 2p$, p being the number of bipolar transistors.

2^{2p}, where p is the number of bipolar transistors. Therefore, this bound appears to be double-exponential in p. The paper [19] does not contain a proof of Theorem 1.

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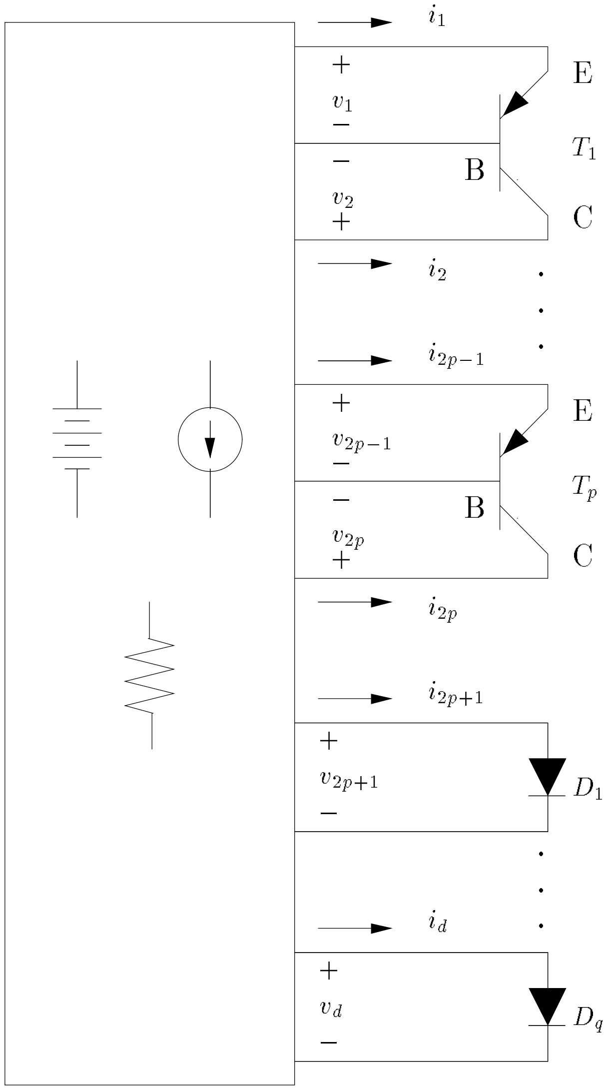

Fig. 1. DC network with bipolar junction transistors. Voltages v_i across transistor pn junctions correspond to the variables x_i.

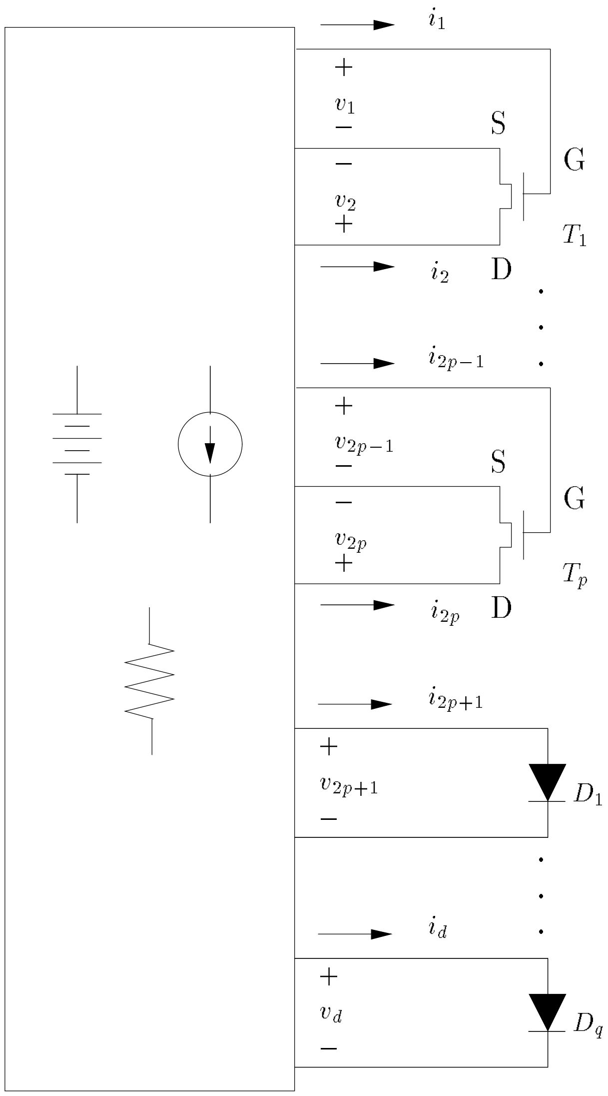

Fig. 2. DC network with field-effect transistors. Voltages v_i across the transistor terminals correspond to the variables x_i.