Power Flow Characterization of a Bidirectional Galvanically Isolated High-Power DC/DC Converter Over a Wide Operating Range

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***Abstract*—This paper studies the power flow characterization of a bidirectional galvanically isolated high-power dual active bridge dc/dc converter. In experimental tests at the University of Michigan, we have observed three phenomena, which we term as internal power transfer, phase drift, and low system efficiency, that are present under certain operating conditions. These phenomena cannot be explained by conventional power transfer analysis. The authors develop a new model, based on a detailed analysis over a short time scale, that incorporates additional parameters, including the power semiconductor voltage loss and dead time. The new power flow model may be used to explain the observed phenomena and to characterize the power flow of the converter. The model may also be used to perform accurate power flow computations over a wide operating range, thereby supporting optimal hardware design, operating range selection, and power management strategy development. Experimental results are presented to illustrate the validity of the new model.**

***Index Terms*—Bidirectional dc/dc converter, dual active bridge (DAB), phase shift modulation, power flow characterization.**

I. Introduction

THE bidirectional galvanically isolated dual active bridge (DAB) dc/dc converter was initially proposed in [1] and [2] for both high power density and high-power applications. Fig. 1 depicts the configuration of the power stage of a DAB dc/dc converter, where D_1–D_8 are the corresponding antiparallel diodes of the power switches Q_1–Q_8, L is the leakage inductor of the transformer with turn ratio n, and C_1 and C_2 are the capacitors connected to the dc side of each bridge. The ac side of each bridge is connected to the transformer with corresponding primary voltage $V_{\rm ac1}$ and secondary voltage $V_{\rm ac2}$, respectively. If we ignore the power semiconductors' voltage loss, $V_{\rm ac1}$ could equal V_1, $-V_1$, or 0, while $V_{\rm ac2}$ could equal V_2, $-V_2$, or 0, depending on the DAB's operating mode, where V_1 and V_2 are the voltages across the capacitors C_1 and C_2, respectively. Unlike many bidirectional isolated dc/dc converters with asymmetrical topology [3]–[9], the DAB converter has two symmetrical full bridges that generate phase shifted transition square waves

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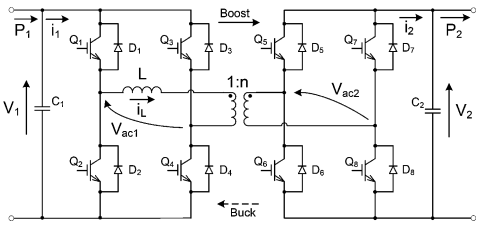


Fig. 1. Isolated bidirectional dc/dc converter topology.

to the transformer's primary and secondary sides. The corresponding phase shift changes the voltage across the transformer leakage inductor, which serves as the main energy transfer element, to manipulate the power flow direction and magnitude. The DAB topology is very attractive because of its zero-voltage switching, bidirectional power flow, low component stresses, and high-power density features [1], [2].

The DAB dc/dc converter has been widely used in applications such as uninterruptible power supplies (UPS), battery charging and discharging systems, and auxiliary power supplies for hybrid electrical vehicles. For example, in [10], the authors investigated an off-line UPS design based on DAB topology. The use of DAB converters for bidirectional energy delivery between an energy storage system and a dc power system is addressed in [11]–[14]. The authors in [15]–[18] evaluate different DAB configurations for automotive applications. The authors in [19]–[21] adopt a DAB converter as the core circuit of the power conversion system between an ac power system and a dc voltage source.

For applications such as energy storage systems, DAB converters are expected to operate over a wide range of operating conditions without substantial performance degradation, especially for mobile applications. To investigate the power flow characterization of the DAB converter, an experimental testbed was developed at the University of Michigan by the authors to support model development and to facilitate power management strategy optimization. The parameters of the DAB converter are shown in Table I. Our experiments revealed three phenomena that are not predicted by the conventional model. These phenomena are internal power transfer at zero phase shift, phase drift, and low system efficiency in certain operating ranges. We now describe each in detail.

The internal power transfer phenomenon refers to nonzero power transfer for zero phase shift. Fig. 2 shows the measured power on both ports (P_1 and P_2) and the calculated P_2 using the conventional power transfer model [1], [2]. It should be noted that the difference between the measured power (P_1 and P_2)

TABLE I
PARAMETERS OF THE DAB CONVERTER PROTOTYPE

Item	Parameter
Inductor L	$9.5uH$
Transformer turn ratio n	2
Switching period T	$100\mu s$
Dead time T_d	$2.5\mu s$
V_1	$30\sim50V$
V_2	$80V$
Rated power	$1000W$

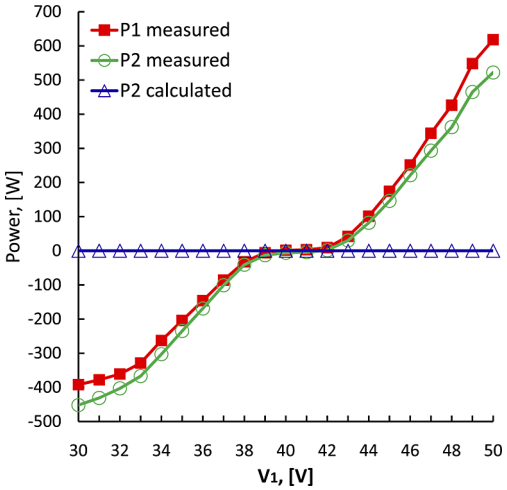


Fig. 2. Internal power transfer for phase shift $= 0$.

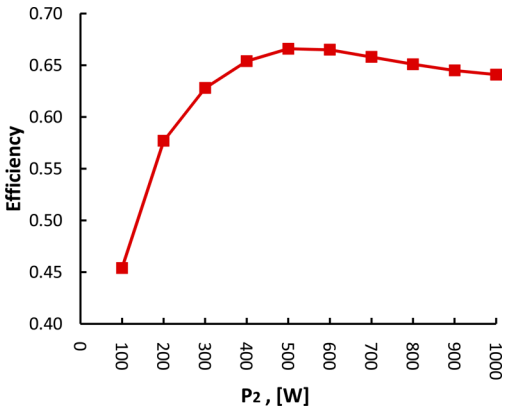


Fig. 3. Measured efficiency curve for $V_1 = 30$.

and the calculated power (P_2) is remarkable and the difference increases as $|nV_1 - V_2|$ increases. A similar phenomenon has been pointed out in [19], where it is referred to as the dead-time[1] negative feedback effect.

Fig. 3 shows the measured efficiency curve of the DAB converter operating with $V_1 = 30$ V and $V_2 = 80$ V. The maximum efficiency is less than 67% for this case. It is known that the negative power leads to high conduction loss, and therefore, reduces the efficiency [12]. However, analytical explanation of

[1]The dead time is a short time period between the modulation sequences of each pair of power switches on the same half bridge, e.g., between Q_1 and Q_2. The dead time is typically used to avoid short-through circuit instead of transferring power.

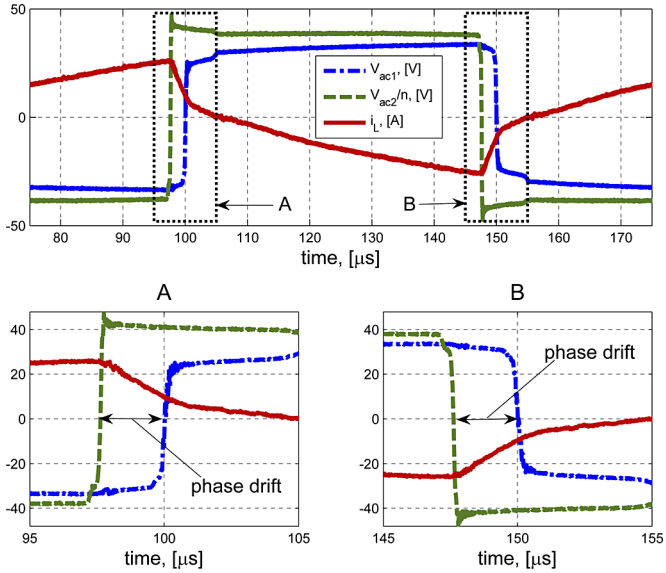


Fig. 4. Phase drift phenomenon for $V_1 = 30$ and phase shift $= 0$. (The two plots at the bottom are zoomed in characteristics of the top one.)

the conditions associated with the low system efficiency has not been fully explored yet.

In addition, the phase drift phenomenon has been observed in experimental tests when $nV_1 \neq V_2$ and the commanded phase shift is zero. As shown in Fig. 4, a phase drift can be identified when zoomed in for the transients between the voltage waveforms $V_{\rm ac1}$ and $V_{\rm ac2}/n$ while the desired phase difference is zero. The phase drift typically imposes a large voltage (with absolute value $\simeq V_{\rm ac1} + V_{\rm ac2}/n \simeq V_1 + V_2/n$) across the inductor and significantly influences the inductor current i_L, as shown in Fig. 4. Therefore, it causes additional power transfer.

Conventional power transfer analysis only considers the *major parameters*, namely the input voltage, output voltage, transformer turn ratio, transformer leakage inductance, switching period, and phase shift. It cannot explain the three phenomena described earlier, thereby motivating an in-depth power flow analysis of the DAB converter on the short time scale.

In this paper, we analytically explain the aforementioned phenomena and characterize the power flow of the DAB converter over a wide operating range. The in-depth analysis on a short time scale leads to a new analytical power transfer model that captures the power flow characteristics over a wide operating range by accounting for not only the major parameters but also additional ones, namely the power semiconductor voltage loss and dead time. Typically, the power semiconductor voltage loss is much smaller than the input and output voltages and the dead time only lasts less than 5% of the switching period. Therefore, these additional parameters are referred to as the *minor parameters* in the rest of paper to distinguish from the aforementioned major ones. We will justify that the minor parameters are critical for explaining the observed three phenomena and characterizing the power flow model of the DAB converter. The new model provides a physical interpretation of the observed phenomena and identifies other characteristics that are validated by experiments. This model also could be used as a design and analysis

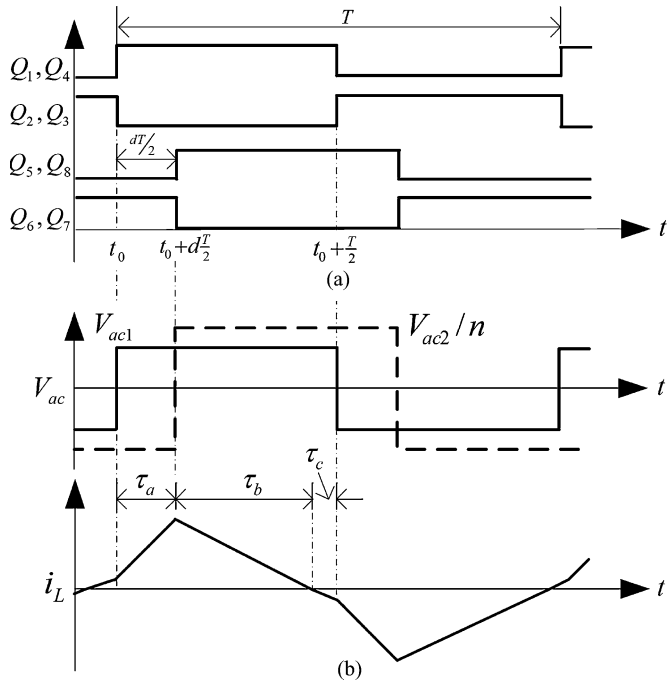


Fig. 5. Phase shift modulation of DAB converter. (a) Modulation sequence. (b) Ideal voltage and current waveforms.

tool to support optimal hardware design and operating range selection.

The rest of this paper is organized as follows. In Section II, the approach used in conventional power flow analysis will be presented. Section III is devoted to analyzing the effects of the minor parameters on power flow. Section IV focuses on power flow characterization over a wide operating range. Section V will be devoted to model validation through experimental results, followed by conclusions in Section VI.

II. Conventional Power Flow Analysis

The DAB dc/dc converter is typically modulated by the phase shift modulation strategy shown in Fig. 5(a). Note that d is the normalized phase shift between the two full bridges. It serves as the control input for manipulating the DAB converter, where $d \in [0, 1]$ for the boost direction and $d \in [-1, 0]$ for the buck direction. Note that since the parallel resistance and inductance are much greater than the series resistance and inductance, the equivalent circuit model of a high-frequency transformer can be simplified as an ideal transformer with primary series inductor (leakage inductor). Therefore, the electrical connection between $V_{\rm ac1}$ and $V_{\rm ac2}$ shown in Fig. 1 can be expressed by the diagram shown in Fig. 6, where L is the leakage inductance. By shifting the phase between the two full bridges, different combinations of $V_{\rm ac1}$ and $V_{\rm ac2}$ can be applied to shape the current i_L, and consequently to manipulate the direction and magnitude of the power flow. The goal of power flow analysis is to obtain an analytical power transfer equation that relates the power flow to the specified power circuit parameters and the phase shift [1], [2]. It is worthwhile to point out that the power flow analysis for both boost and buck directions is essentially the same because of the symmetric structure of the DAB converter. Therefore, for

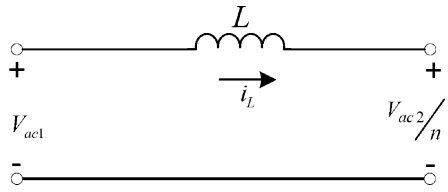


Fig. 6. Simplified dc/dc converter scheme.

conciseness, only the boost direction will be investigated in the subsequent analysis.

Since the dynamics of the capacitor voltages V_1 and V_2 are much slower than that of the inductor current i_L, we can assume that V_1 and V_2 are constant over each switching period. Therefore, to compute the average power, we can define operating modes according to the evolution of i_L. Whenever the inductor current i_L either changes slope or crosses zero, the operating mode changes. Consider the case $nV_1 < V_2$ as an example. For the half switching period $[t_0, t_0 + (T/2)]$, there are three operating modes, namely $\mathcal{M}_1$, $\mathcal{M}_2$, and $\mathcal{M}_3$ with corresponding time intervals τ_a, τ_b, and τ_c, respectively, as illustrated in Fig. 5(b), where

$$\mathcal{M}_1 : \ t \in [t_0, t_0 + \tau_a]$$
$$\mathcal{M}_2 : \ t \in [t_0 + \tau_a, t_0 + \tau_a + \tau_b]$$
$$\mathcal{M}_3 : \ t \in \left[t_0 + \tau_a + \tau_b, t_0 + \frac{T}{2}\right].$$

Note that $\tau_a + \tau_b + \tau_c = T/2$. It is also worthwhile to point out that, for all waveforms of $V_{\rm ac}$, i_L, i_1, and i_2 presented in figures of this paper, the time-axis intersects the y-axis at $y = 0$.

If we ignore the difference between the input and output power and only consider the major parameters, namely V_1, V_2, n, T, and L, we have

$$V_{\rm ac1} - \frac{V_{\rm ac2}}{n} = L\frac{di_L}{dt} = \begin{cases} V_1 + \dfrac{V_2}{n}, & \text{for } \mathcal{M}_1 \\ V_1 - \dfrac{V_2}{n}, & \text{for } \mathcal{M}_2 \text{ and } \mathcal{M}_3. \end{cases} \tag{1}$$

Given the symmetric structure of the DAB converter topology, at steady state, the average value of $i_L(t)$ must be zero over one switching period T and $i_L(t_0) = -i_L(t_0 + (T/2))$.

Therefore

$$i_L\left(t_0 + \frac{T}{2}\right) = \frac{(nV_1 - V_2)\tau_c}{nL} = -i_L(t_0) \tag{2}$$

$$i_L\left(t_0 + d\frac{T}{2}\right) = -\frac{(nV_1 - V_2)\tau_b}{nL} = \frac{(nV_1 + V_2)\tau_a}{nL} + i_L(t_0). \tag{3}$$

Equations (2) and (3) lead to

$$\frac{(nV_1 + V_2)\tau_a}{nL} + \frac{(nV_1 - V_2)\tau_b}{nL} - \frac{(nV_1 - V_2)\tau_c}{nL} = 0. \tag{4}$$

Note that

$$\tau_a = \frac{dT}{2}, \qquad \tau_a + \tau_b + \tau_c = \frac{T}{2}. \tag{5}$$

Solving (4) and (5), we have

$$\tau_b = \frac{(nV_1 - V_2) - 2nV_1 d}{2(nV_1 - V_2)} \frac{T}{2} \tag{6}$$

$$\tau_c = \frac{(nV_1 - V_2) + 2V_2 d}{2(nV_1 - V_2)} \frac{T}{2}. \tag{7}$$

With the assumption that the input and output voltages V_1 and V_2 are constant over one switching period, the average output power P_2 can be calculated as

$$\begin{aligned} P_2 &= \frac{2}{T}\int_{t_0}^{t_0+T/2} V_1 i_L \, dt = V_1 \times \frac{2}{T}\int_{t_0}^{t_0+T/2} i_L \, dt \\ &= \frac{2V_1}{T}\left\{ \frac{i_L(t_0 + (T/2))(\tau_c - \tau_a)}{2} \right. \\ &\qquad \left. + \frac{i_L(t_0 + (dT/2))(\tau_a + \tau_b)}{2} \right\} \\ &= \frac{TV_1V_2 d(1-d)}{2nL}. \end{aligned} \tag{8}$$

Remark 1: At zero phase shift ($d = 0, \tau_a = dT/2 = 0$), we have

1) $\tau_b = \tau_c = T/4$;
2) the slopes of i_L are the same over the two modes $\mathcal{M}_2$ and $\mathcal{M}_3$[2];
3) the average current of $\hat{i}_L = (2/T)\int_{t_0}^{t_0+(T/2)} i_L \, dt = 0$, therefore $P_2 = 0$.

Note that for $nV_1 \geq V_2$, the power flow expression is the same as (8) [1], [2].

Remark 2: We define the power in the desired direction as the positive power and the power in the opposite direction as the negative power. Equation (8) and Remark 1 suggest that, for zero phase shift, the positive power and the negative power are canceled over the half switching cycle if we only consider the major parameters. Therefore, the average output power is always zero. This conclusion contradicts with the experimental results shown in Fig. 2, motivating an in-depth power flow analysis for the DAB converter (to be presented in the subsequent sections).

III. Effects of Minor Parameters on Power Transfer of DAB Converter

Traditional power flow analysis for power converters only considers major parameters [22]. This is because most power converters use a dedicated inductor as the energy transfer element, and the input or output voltage is directly applied to the inductor. Therefore, the voltage loss of the power semiconductor is negligible. However, the DAB converter uses a microhenry- or even nanohenry-level leakage inductor as the energy transfer element. The voltage applied to the inductor depends on $|V_{\rm ac1} + V_{\rm ac2}/n|$ and $|V_{\rm ac1} - V_{\rm ac2}/n|$ for different time intervals. For many applications [11], [12], $|V_{\rm ac1} - V_{\rm ac2}/n|$ is only several volts, which leads to the hypothesis that the power semiconductor voltage loss is not negligible for the power flow characterization of the DAB converter. On the other hand, the phase drift phenomenon and internal power transfer phenomenon are correlated to the dead time in experimental results. Dead time typically causes additional output voltage deviation and power loss for power converters [23], [24]. Therefore, an analysis of the dead-time effect is necessary for understanding the phase drift phenomenon. In the following subsections, in addition to major parameters V_1, V_2, L, T, n, and d used in the conventional analysis, we investigate the effects of the minor parameters, namely power semiconductor voltage loss and dead time.

[2]This property holds for all $d \in [0, 1]$ by (1).

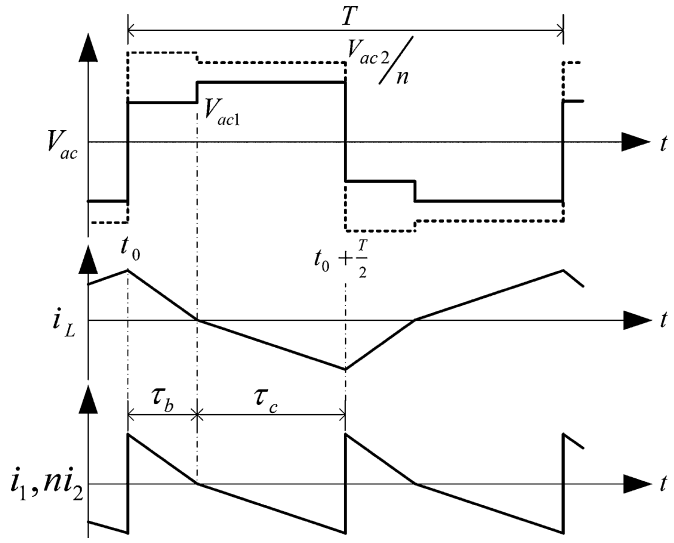


Fig. 7. Ideal waveforms of DAB converter considering power semiconductor voltage loss.

TABLE II
Voltage Across the Leakage Inductor Considering Power Semiconductors Voltage Loss

Operating mode	V_{ac1}	V_{ac2}
$\mathcal{M}_2$	$V_1 - 2V_s$	$V_2 + 2V_d$
$\mathcal{M}_3$	$V_1 + 2V_d$	$V_2 - 2V_s$

A. Power Semiconductor Voltage Loss Effect

To illustrate the effects of voltage loss across power switches, we again consider the case $nV_1 < V_2$ and $d = 0$. The ideal waveforms are shown in Fig. 7. Let V_s and V_d denote the voltage loss across the power switches Q_1–Q_8 and antiparallel diodes D_1–D_8. Note that, for conciseness, we assume that the power switches and antiparallel diodes of the primary full bridge have the same voltage loss as their corresponding counterparts of the secondary full bridge. In general, the voltage loss of a power semiconductor may not be constant for varying current. However, for a given operating range, it is reasonable to assume constant voltage loss because the conduction resistance of the power semiconductor is very small (in milliohm level). We now proceed to characterize the power flow of the DAB converter as follows.

Define $\mathcal{M}_1$, $\mathcal{M}_2$, and $\mathcal{M}_3$ in the same way as in Section II (now $\tau_a = 0$ since $d = 0$), where the voltages across the leakage inductor at different time intervals are given in Table II.

Given that $i_L(t_0) = -i_L(t_0 + T/2)$, we have

$$\frac{\tau_b}{\tau_c} = \frac{nV_1 + 2nV_d - (V_2 - 2V_s)}{nV_1 - 2nV_s - (V_2 + 2V_d)}. \tag{9}$$

Equation (9) together with

$$\tau_a = 0, \qquad \tau_a + \tau_b + \tau_c = \frac{T}{2} \tag{10}$$

will give

$$\tau_b = \frac{nV_1 - V_2 + 2nV_d + 2V_s}{2nV_1 - 2V_2 - 2(n-1)(V_s - V_d)} \frac{T}{2} \tag{11}$$

$$\tau_c = \frac{nV_1 - V_2 - 2nV_s - 2V_d}{2nV_1 - 2V_2 - 2(n-1)(V_s - V_d)} \frac{T}{2}. \tag{12}$$

Moreover

$$i_1(t) = ni_2(t) = \begin{cases} i_L(t), & t \in [t_0, t_0 + \frac{T}{2}] \\ -i_L(t), & t \in [t_0 + \frac{T}{2}, t_0 + T]. \end{cases} \tag{13}$$

$$i_L\left(t_0 + \frac{T}{2}\right) = \frac{(nV_1 - V_2 + 2nV_d + 2V_s)\tau_c}{nL}. \tag{14}$$

Therefore, the average power can be calculated as

$$P_1 = \frac{2}{T}\int_0^{T/2} V_1 i_1 \, dt = \frac{2V_1}{T}\left\{\frac{i_L(t_0 + (T/2))(\tau_c - \tau_b)}{2}\right\} \tag{15}$$

$$P_2 = \frac{2}{T}\int_0^{T/2} V_2 i_2 \, dt = \frac{2V_2}{TV_1}\int_0^{T/2} V_1 \frac{i_1}{n} \, dt = \frac{P_1 V_2}{nV_1}. \tag{16}$$

Remark 3: At zero phase shift, the voltage loss of the power semiconductor can cause:

1) $\tau_b \neq \tau_c$ [as shown by (9)];
2) the slope of i_L is not the same for modes $\mathcal{M}_2$ and $\mathcal{M}_3$, since the voltage across the inductor $V_{\mathrm{ac1}} - V_{\mathrm{ac2}}/n$, calculated using data in Table II, are different;
3) $P_1 \neq 0$ and $P_2 \neq 0$ as calculated in (15) and (16).

Therefore, the minor parameters V_s and V_d affect the distribution of positive power and negative power, leading to $P_1 \neq 0$ and $P_2 \neq 0$ at $d = 0$. Taking this one step further, the effects of dead time will be considered in the next section.

B. Dead-Time Effect

We now show that the existence of a dead time causes the phase drift phenomenon we noted in the Section I. For continuity and simplicity, we consider again the case with $nV_1 < V_2$ and $d = 0$. Referring to the current and voltage waveforms plotted in Fig. 8, suppose that the DAB is modulated by gating sequences V_g, with dead time T_d between transits at each half switching period. Given $nV_1 < V_2$, $i_L(t)$ must be decreasing during $t_0 \leq t \leq t_0 + (T/2)$, since Q_1, Q_4, Q_5, and Q_8 are turned on and $V_{\mathrm{ac1}} > 0$, $V_{\mathrm{ac2}} > 0$. Given the symmetric structure of the topology, $i_L(t_0) = -i_L(t_0 + T/2)$, we must have $i_L(t_0) > 0$ and $i_L(t_0 + (T/2)) < 0$, implying that i_1 has to pass through D_1 and D_4 while i_2 passes through Q_5 and Q_8 during τ_c. At time $t = t_0 + (T/2)$, Q_1, Q_4, Q_5, and Q_8 are turned off, causing i_2 to be switched to D_6 and D_7 immediately while i_1 keeps passing through D_1 and D_4. This is equivalent to an undesired additional phase shift between V_{ac1} and V_{ac2}, which enables i_1 passing the power devices Q_1/D_1 and Q_4/D_4 during the dead time. We define the undesired phase shift as *phase drift*. If $i_L(t_0 + (T/2))$ is not large enough, then $i_L(t)$ will go to zero before $t = t_0 + (T/2) + T_d$, as shown in Fig. 8(a) (Case I), meaning that there is a negative phase drift $\in [-2T_d/T, 0]$. Otherwise, i_1 keeps passing through D_1 and D_4 until the dead time ends and Q_2 and Q_3 are turned on, as shown in Fig. 8(b) (Case II), leading to a negative phase drift $-2T_d/T$. Similarly, for the case $nV_1 > V_2$ and $d = 0$, there is a phase drift (lead) for the primary voltage V_{ac1} in comparison with the secondary voltage V_{ac2}.

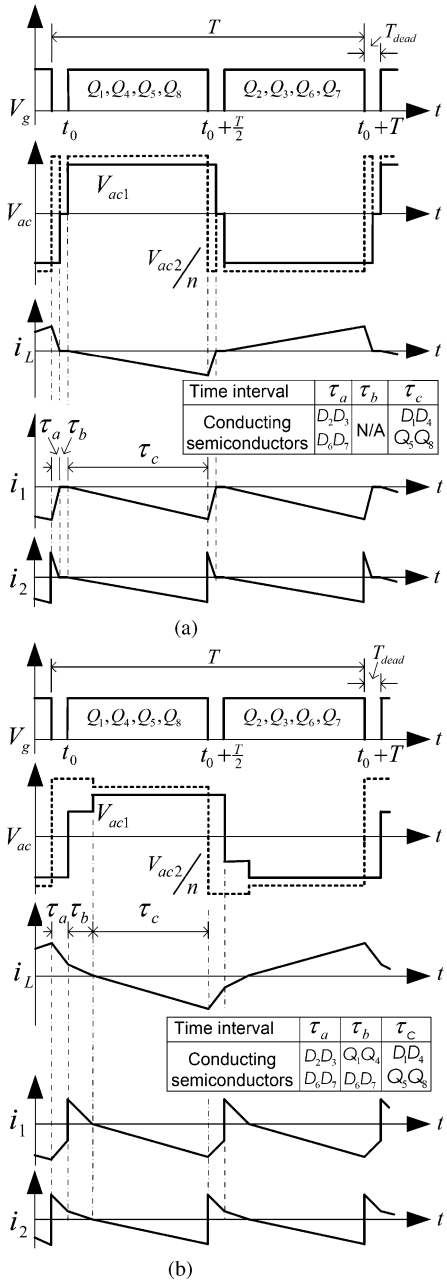


Fig. 8. Dead-time effect of DAB converter.

TABLE III
VOLTAGE ACROSS THE LEAKAGE INDUCTOR FOR CASE I

Operating mode	V_{ac1}	V_{ac2}
$\mathcal{M}_1$	$-(V_1+2V_d)$	V_2+2V_d
$\mathcal{M}_3$	V_1+2V_d	V_2-2V_s

Remark 4: The phase drift only provides the freewheeling path for the inductor current i_L and i_L can reach zero but never can cross zero and be built up.

We next derive expressions for the power flow that include the dead time as well as the voltage loss.

1) Case I: If $|V_{\rm ac1}-V_{\rm ac2}/n|$ is not large enough to build large $|i_L|$, then $|i_L|$ reduces to zero before $t=t_0+(T/2)+T_d$, which results in a phase drift $\in[-2T_d/T,0]$. In this case, the ideal waveforms are shown in Fig. 8(a). Define $\mathcal{M}_1$, $\mathcal{M}_2$, and $\mathcal{M}_3$ in the same way as in Section II, where the voltages across the leakage inductor at different time intervals are shown in Table III. Here, $\mathcal{M}_2$ is not considered given that $i_L=0, i_1=0$, and $i_2=0$ for $t\in\mathcal{M}_2$.

From Table III and

$$\tau_c=\frac{T}{2}-T_d. \tag{17}$$

we can derive

$$\tau_a=\frac{nV_1-V_2+2nV_d+2V_s}{nV_1+V_2+2(n+1)V_d}\tau_c \tag{18}$$

$$i_L\left(t_0+\frac{T}{2}\right)=\frac{(nV_1-V_2+2nV_d+2V_s)\tau_c}{nL}. \tag{19}$$

Moreover

$$i_1(t)=\begin{cases}-i_L(t), & \text{for } t\in[t_0,t_0+\tau_a]\\ i_L(t), & \text{for } t\in[t_0+\tau_a,t_0+T/2+\tau_a]\\ -i_L(t), & \text{for } t\in[t_0+T/2+\tau_a,t_0+T].\end{cases} \tag{20}$$

$$i_2(t)=\begin{cases}\dfrac{i_L(t)}{n}, & \text{for } t\in[t_0,t_0+T/2]\\ -\dfrac{i_L(t)}{n}, & \text{for } t\in[t_0+T/2,t_0+T].\end{cases} \tag{21}$$

Therefore, the average powers, P_1 and P_2, are

$$\begin{aligned}P_1&=\frac{2}{T}\int_0^{T/2}V_1i_1\,dt\\&=\frac{2V_1}{T}\left\{\frac{i_L(t_0+(T/2))(\tau_a+\tau_c)}{2}\right\}.\end{aligned} \tag{22}$$

$$\begin{aligned}P_2&=\frac{2}{T}\int_0^{T/2}V_2i_2\,dt\\&=\frac{2V_2}{nT}\left\{\frac{i_L(t_0+(T/2))(\tau_c-\tau_a)}{2}\right\}.\end{aligned} \tag{23}$$

Note that, for case I, $|i_L|$ reduces to zero before $t=t_0+(T/2)+T_d$. This fact implies $\tau_a+\tau_c\le T/2$. Therefore, for $\tau_b=T/2-\tau_a-\tau_c$, there is no power transfer ($i_L=0$).

2) Case II: If $|V_{\rm ac1}-V_{\rm ac2}/n|$ is large enough to build large $|i_L|$ such that $i_L(t_0+(T/2)+T_d)\neq 0$, then the phase drift equals to $-2T_d/T$. In this case, the ideal waveforms are shown in Fig. 8(b). Defining $\mathcal{M}_1$, $\mathcal{M}_2$, and $\mathcal{M}_3$ as in Section II, the voltages across the leakage inductor at different time intervals are shown in Table IV.

TABLE IV
VOLTAGE ACROSS THE LEAKAGE INDUCTOR FOR CASE II

Operating mode	V_{ac1}	V_{ac2}
$\mathcal{M}_1$	$-(V_1+2V_d)$	V_2+2V_d
$\mathcal{M}_2$	V_1-2V_s	V_2+2V_d
$\mathcal{M}_3$	V_1+2V_d	V_2-2V_s

Given Table IV and

$$\tau_a=T_d \tag{24}$$

$$\tau_a+\tau_b+\tau_c=\frac{T}{2} \tag{25}$$

we can derive

$$\tau_b=\frac{(nV_1-V_2+2nV_d+2V_s)\frac{T}{2}+2(V_2+V_d-V_s)T_d}{2nV_1-2V_2-2(n-1)(V_s-V_d)} \tag{26}$$

$$\tau_c=\frac{(nV_1-V_2-2V_d-2nV_s)\frac{T}{2}-2n(V_1+V_d-V_s)T_d}{2nV_1-2V_2-2(n-1)(V_s-V_d)}. \tag{27}$$

Moreover

$$i_1(t)=\begin{cases}-i_L(t), & \text{for } t\in[t_0,t_0+\tau_a]\\ i_L(t), & \text{for } t\in[t_0+\tau_a,t_0+T/2+\tau_a]\\ -i_L(t), & \text{for } t\in[t_0+T/2+\tau_a,t_0+T].\end{cases} \tag{28}$$

$$i_2(t)=\begin{cases}\dfrac{i_L(t)}{n}, & \text{for } t\in[t_0,t_0+T/2]\\ -\dfrac{i_L(t)}{n}, & \text{for } t\in[t_0+T/2,t_0+T].\end{cases} \tag{29}$$

$$i_L(t_0+T_d)=\frac{-(nV_1-V_2-2V_d-2nV_s)\tau_b}{nL} \tag{30}$$

$$i_L\left(t_0+\frac{T}{2}\right)=-i_L(t_0)=\frac{(nV_1-V_2+2nV_d+2V_s)\tau_c}{nL}. \tag{31}$$

Therefore, the average power P_1 and P_2 are

$$\begin{aligned}P_1&=\frac{2}{T}\int_0^{T/2}V_1i_1\,dt\\&=\frac{2V_1}{T}\left\{\frac{i_L(t_0+(T/2))(\tau_a+\tau_c)}{2}+\frac{i_L(t_0+T_d)(\tau_b-\tau_a)}{2}\right\}.\end{aligned} \tag{32}$$

$$\begin{aligned}P_2&=\frac{2}{T}\int_0^{T/2}V_2i_2\,dt\\&=\frac{2V_2}{nT}\left\{\frac{i_L(t_0+(T/2))(\tau_c-\tau_a)}{2}+\frac{i_L(t_0+T_d)(\tau_a+\tau_b)}{2}\right\}.\end{aligned} \tag{33}$$

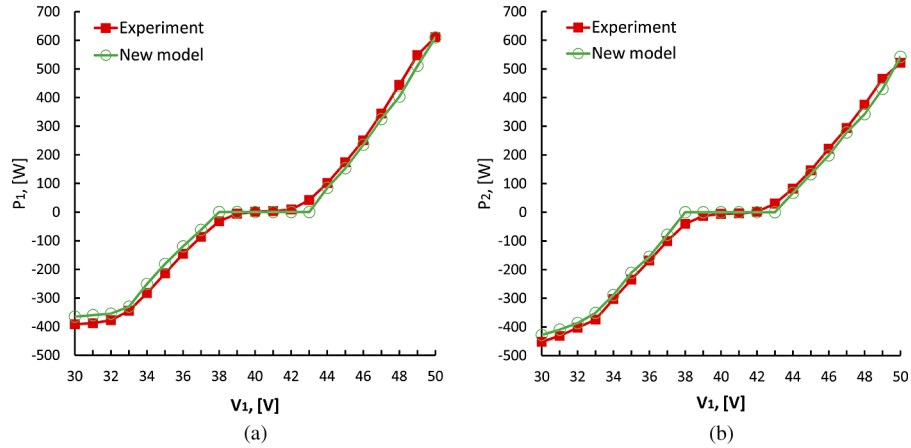


Fig. 9. Power flow model validation for $V_2 = 80$ V and $d = 0$. (a) P_1. (b) P_2.

Similarly, for the case of $nV_1 > V_2$ and $d = 0$, a model for P_1 and P_2 can be derived in the same manner. Given the symmetric structure of the DAB converter, the analysis is also valid for the buck direction ($d \in [-1, 0]$).

Note that for the case of $d \neq 0$, *Case I* and *Case II* can be combined. This is because small d can build up $|i_L|$ such that $i_L(t_0 + (T/2) + T_d) \neq 0$, resulting in a phase drift equal to $-2T_d/T$.

Remark 5: The dead-time effect analysis for $d = 0$ can be extended to $d \neq 0$. Let t_0 donate the time instance when the transformer primary voltage V_{ac1} changes polarity to positive. Then, if $i_L(t_0 + (T/2)) \times i_L(t_0 + (T/2) + (dT/2)) > 0$, there is a phase drift between V_{ac1} and the transformer secondary voltage V_{ac2}. More specifically, if $i_L(t_0 + (T/2)) < 0$, $i_L(t_0 + (T/2)) \times i_L(t_0 + (T/2) + (dT/2)) > 0$ implies $i_L(t_0 + (T/2) + (dT/2)) < 0$. Therefore, i_L can be immediately switched to different power devices at $t = t_0 + (T/2) + (dT/2)$ while i_L has to pass through the original devices at $t = t_0 + (T/2)$ until the end of the dead time, leading to a negative phase shift $-2T_d/T$; similarly, if $i_L(t_0 + (T/2)) > 0$, there is a positive phase shift $2T_d/T$. Moreover, if the DAB converter operates in a small d region, then there is a phase drift because a small d leads to $i_L(t_0 + (T/2)) \times i_L(t_0 + (T/2) + (dT/2)) > 0$. Moreover, if $i_L(t_0 + (T/2)) \times i_L(t_0 + (T/2) + (dT/2)) < 0$, there is no phase drift between V_{ac1} and V_{ac2}. This is because i_L can be immediately switched to different power devices at $t = t_0 + (T/2)$ and $t = t_0 + (T/2) + (dT/2)$ if $i_L(t_0 + (T/2)) \times i_L(t_0 + (T/2) + (dT/2)) < 0$.

Fig. 9 shows that the calculated P_1 and P_2 based on the analysis presented in this section are very close to the experimental results. Therefore, the minor parameters V_s, V_d, and T_d affect the slope of i_L and the length of the time intervals τ_a, τ_b, and τ_c, and consequently influence the distribution of positive power and negative power as well as the average power P_1 and P_2. The effectiveness of the results for $d = 0$ (see Fig. 9) and the extension of dead-time effect analysis to $d \neq 0$ (see Remark 5) motivate the authors to explore power flow characterization of the DAB converter over a wide operating range, which will be discussed in the next section.

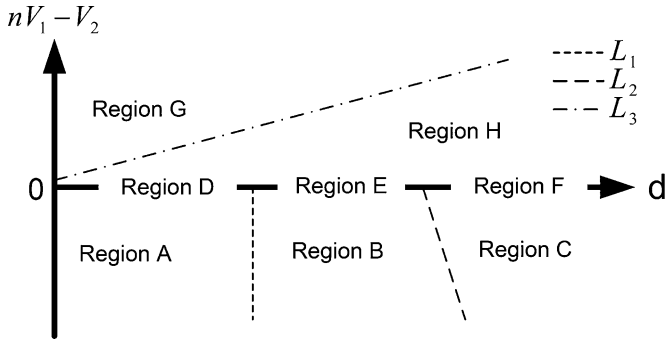


Fig. 10. Operating region separation.

IV. Power Flow Characterization of DAB DC/DC Converter Over Wide Operating Range

We now derive a general characterization for the power flow of the DAB converter. To do so, we consider three different cases, namely $nV_1 < V_2$, $nV_1 = V_2$, and $nV_1 > V_2$, because $V_{\mathrm{ac1}} + V_{\mathrm{ac2}}/n \simeq V_1 + V_2/n$ and $V_{\mathrm{ac1}} - V_{\mathrm{ac2}}/n \simeq V_1 - V_2/n$ determine the shape of i_L. For each case, we divide the operating range $d \in [0, 1]$ of the converter into several regions, which is defined as illustrated in Fig. 10 and described in detail shortly. For different operating regions, Fig. 11 shows the corresponding ideal waveforms of the DAB converter, while Table V lists all necessary equations for deriving the boundaries and the power flow equations for different regions. The following intermediate variables are defined in order to present Table V:

$$K_1 = nV_1 - V_2 + 2nV_d + 2V_s \tag{34}$$

$$K_2 = nV_1 - V_2 - 2nV_s - 2V_d \tag{35}$$

$$K_3 = 2n(V_1 + V_d - V_s) \tag{36}$$

$$K_4 = 2(V_2 + V_d - V_s) \tag{37}$$

$$K_5 = nV_1 + V_2 - 2(n+1)V_s \tag{38}$$

$$K_6 = nV_1 + V_2 + 2(n+1)V_d \tag{39}$$

$$K_7 = 2nV_1 - 2V_2 - 2(n-1)(V_s - V_d) \tag{40}$$

$$K_8 = 2nV_1 - 2V_2 - 2(n+1)(V_s - V_d) \tag{41}$$

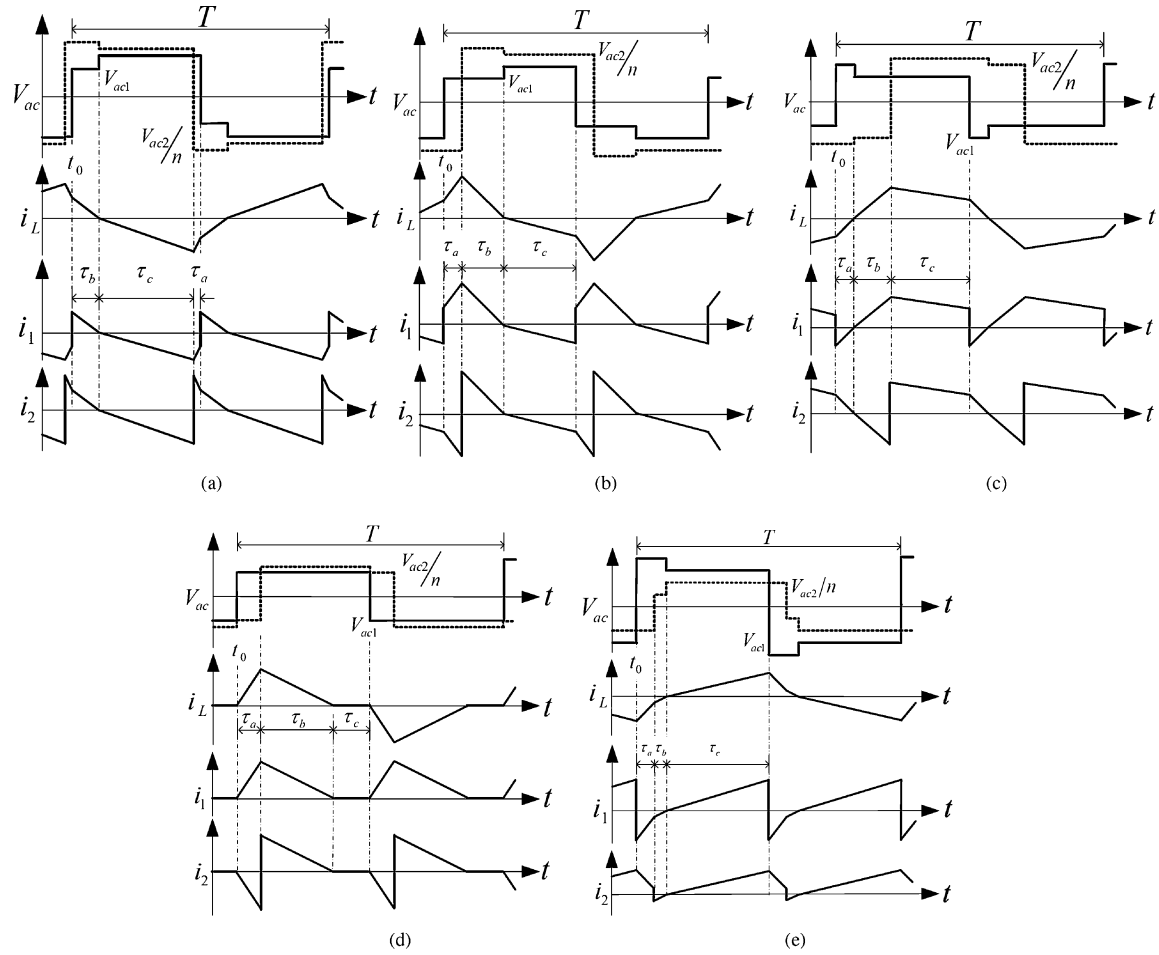


Fig. 11. Ideal waveforms for DAB converter with phase shift modulation strategy. (a) Region A. (b) Region B. (c) Region C. (d) Region E. (e) Region G.

$$i_3 = i_L(t_0) \tag{42}$$

$$i_4 = i_L(t_0 + \tau_a) \tag{43}$$

$$i_5 = i_L(t_0 + \tau_a + \tau_b). \tag{44}$$

We now describe each of these regions in detail.

For $nV_1 < V_2$, referring to Fig. 11(a) or (b) and Table V (region A or B), $i_L(t_0) > 0$ while $i_L(t_0 + (T/2)) < 0$ if the converter operates in a small d region. Moreover, $i_L(t_0 + (T/2) + (dT/2)) < 0$ for a small d. Therefore, following Remark 5, there is a phase drift $\delta = -2T_d/T$ over a certain range of d. So, the DAB converter will be operating with three different regions in this case. The first region (region A) is $0 \le d \le 2T_d/T$, wherein $d + \delta$ is less than zero due to the phase drift. Let $L_1 = 2T_d/T$ represent the boundary line between regions A and B. In region B, the phase drift phenomenon still exists, but the actual phase shift is larger than zero. However, referring to Fig. 11(b) and Table V (region B), τ_c decreases as d increases. If $d = -(nV_1 - V_2 - 2V_d - 2nV_s)/2(V_2 + V_d - V_s) + 2T_d/T$, $i_L(t_0 + (T/2)) = 0$ ($\tau_c = 0$). Let $L_2 = -(nV_1 - V_2 - 2V_d - 2nV_s)/2(V_2 + V_d - V_s) + 2T_d/T$ denote the boundary line between regions B and C, $i_L(t_0 + (T/2)) > 0$ if the converter operates at the right side of the boundary line L_2. Moreover, $i_L(t_0 + (T/2) + (dT/2)) < 0$ in that case, so the current in both bridges can be immediately switched. Therefore, there is no phase drift, thus leading to the third region (region C).

For $nV_1 = V_2$, there is a phase drift $\delta = -2T_d/T$ for small d by as discussed in Remark 5. This is because the DAB converter works with discontinuous current mode (DCM) for small d such that $i_L(t_0 + (T/2)) < 0$ and $i_L(t_0 + (T/2) + (dT/2)) < 0$. Moreover, there is no power transfer if $d \le 2T_d/T$ since $i_L(t_0 + (T/2)) \simeq 0$ and the phase drift only provide freewheeling path for i_L and cannot build up inductor current (Remark 4). The DAB converter operates with continuous current mode (CCM) ($i_L(t_0 + (T/2)) > 0$) for large d, and there is no phase drift. Therefore, three regions are defined in this case. The first region (region D) is defined by $0 \le d \le 2T_d/T$, where there is no power transfer. The DAB converter operates with DCM mode in the second region (region E) wherein $\delta = -2T_d/T$. For $d = (2V_d + 2nV_s)/2(V_2 + V_d - V_s) + 2T_d/T$, referring to Fig. 11(e) and Table V (region E), we have $i_L(t_0 + T/2) = 0$ ($\tau_c = 0$). Since $nV_1 = V_2$, we can use the same boundary line $L_2 = -(nV_1 - V_2 - 2V_d - 2nV_s)/2(V_2 + V_d - V_s) + 2T_d/T$ to represent the boundary line separating regions E and F. If the converter operates at the right side of the boundary line L_2, we have $i_L(t_0 + (dT/2)) > 0$ and

TABLE V
POWER FLOW CHARACTERIZATION TABLE

Region	Mode	V_{ac1}	V_{ac2}	τ_a,τ_b,τ_c	i_3	i_4	i_5	P_1	P_2
A	$\mathcal{M}_1$	$-(V_1+2V_d)$	V_2+2V_d	$T_d-d\frac{T}{2}$	$-\frac{K_1\tau_c}{nL}$	$-\frac{K_2\tau_b}{nL}$	0	$\frac{V_1[i_4(\tau_b-\tau_a)-i_3(\tau_a+\tau_c)]}{T}$	$\frac{V_2[i_4(\tau_b+\tau_a)+i_3(\tau_a-\tau_c)]}{nT}$
	$\mathcal{M}_2$	V_1-2V_s	V_2+2V_d	$\frac{K_1\frac{T}{2}+K_4\tau_a}{K_7}$					
	$\mathcal{M}_3$	V_1+2V_d	V_2-2V_s	$\frac{K_2\frac{T}{2}-K_3\tau_a}{K_7}$					
B	$\mathcal{M}_1$	V_1-2V_s	$-(V_2-2V_s)$	$d\frac{T}{2}-T_d$	$-\frac{K_1\tau_c}{nL}$	$-\frac{K_2\tau_b}{nL}$	0	$\frac{V_1[i_4(\tau_a+\tau_b)+i_3(\tau_a-\tau_c)]}{T}$	$\frac{V_2[i_4(\tau_b-\tau_a)-i_3(\tau_a+\tau_c)]}{nT}$
	$\mathcal{M}_2$	V_1-2V_s	V_2+2V_d	$\frac{K_1\frac{T}{2}-K_3\tau_a}{K_7}$					
	$\mathcal{M}_3$	V_1+2V_d	V_2-2V_s	$\frac{K_2\frac{T}{2}+K_4\tau_a}{K_7}$					
C	$\mathcal{M}_1$	V_1+2V_d	$-(V_2+2V_d)$	$\frac{K_2T/2+K_4dT/2}{K_8}$	$-\frac{K_6\tau_a}{nL}$	0	$\frac{K_5\tau_b}{nL}$	$\frac{V_1[i_5(\tau_b+\tau_c)+i_3(\tau_a-\tau_c)]}{T}$	$\frac{V_2[i_5(\tau_c-\tau_b)-i_3(\tau_a+\tau_c)]}{nT}$
	$\mathcal{M}_2$	V_1-2V_s	V_2-2V_s	$\frac{-K_2\frac{T}{2}+K_3d\frac{T}{2}}{K_8}$					
	$\mathcal{M}_3$	V_1-2V_s	V_2+2V_d	$(1-d)\frac{T}{2}$					
E	$\mathcal{M}_1$	V_1-2V_s	$-(V_2-2V_s)$	$d\frac{T}{2}-T_d$	0	$\frac{K_5\tau_a}{nL}$	0	$\frac{V_1i_4(\tau_a+\tau_b)}{T}$	$\frac{V_2i_4(\tau_b-\tau_a)}{nT}$
	$\mathcal{M}_2$	V_1-2V_s	V_2+2V_d	$-\frac{K_5\tau_a}{K_2}$					
	$\mathcal{M}_3$	V_1-2V_s	V_2+2V_d	$\frac{T}{2}-\tau_a-\tau_c$					
G	$\mathcal{M}_1$	V_1+2V_d	$-(V_2+2V_d)$	$d\frac{T}{2}+T_d$	$-\frac{K_1\tau_b}{nL}$	$\frac{K_2\tau_c}{nL}$	0	$\frac{V_1[i_4(\tau_a+\tau_b)+i_3(\tau_a-\tau_c)]}{T}$	$\frac{V_2[i_4(\tau_a+\tau_b)+i_3(\tau_a+\tau_c)]}{nT}$
	$\mathcal{M}_2$	V_1+2V_d	V_2-2V_s	$\frac{K_2\frac{T}{2}-K_3\tau_a}{K_7}$					
	$\mathcal{M}_3$	V_1-2V_s	V_2+2V_d	$\frac{K_1\frac{T}{2}+K_4\tau_a}{K_7}$					

$i_L(t_0+(T/2)+(dT/2))<0$, leading to the third region (region F) wherein phase drift $\delta=0$.

For $nV_1>V_2$ and small d, the phase drift is $\delta=2T_d/T$ (Remark 5) because $i_L(t_0+(T/2))>0$ and $i_L(t_0+(T/2)+(dT/2))>0$. Therefore, two regions are defined in this case. For the first region (region G), the actual phase shift equals to $d+2T_d/T$. If $d=(nV_1-V_2-2V_d-2nV_s)/2n(V_1+V_d-V_s)-2T_d/T$, then $i_L(t_0+(T/2)+(dT/2))=0$ $(\tau_b=0)$. Let $L_3=(nV_1-V_2-2V_d-2nV_s)/2n(V_1+V_d-V_s)-2T_d/T$ representing the boundary line between regions G and H. If the converter operates at the right side of the boundary line L_3, we have $i_L(t_0+(T/2))>0$ and $i_L(t_0+(T/2)+(dT/2))<0$, leading to the second region (region H) with zero phase drift.

Note that for all of three cases, namely $nV_1<V_2$, $nV_1=V_2$, and $nV_1>V_2$, we assume that the operating mode of the DAB converter will transfer from the region with a phase drift (region B, E, or G) to the corresponding one without phase drift (region C, F, or H) immediately whenever d acroses the boundary lines L_2 and L_3, respectively. But in reality, there will be a short interval wherein the phase drift phenomenon fades away gradually if d acroses the boundary lines. Due to the symmetric structure of the converter, the analysis can be also applied for the buck direction operation.

The power flow analysis for different regions can be performed following the same procedure as presented in Section III. Note that there is no power transfer for region D, and regions F and H have the same power flow characterization as region C. Therefore, only waveforms and equations of regions A, B, C, E, and G are provided in Fig. 11 and Table V.

Remark 6: For different operating regions depicted in Fig. 10, the influence of the minor parameters on operating regions are summarized as follows.

1) Dead time introduces negative phase drift in regions A, B, D, and E and positive phase drift in region G. Dead time has no impact in regions C, F, and H. Moreover, in regions A, B, and G, the converter operates with hard switching since it does not satisfy the soft-switching condition given by De Doneker *et al.* [1]. In addition, phase drift introduces additional negative power over each half switching period in regions A, B, and G, leading to high conduction loss. Furthermore, for high power applications, since the dead time has to be chosen large enough to assure safe operation of the converter, the dead-time effect will be significant if the converter operates in regions A, B, and G. Therefore, the DAB converter should be designed such that the nominal operation point is outside regions A, B, and G to achieve high system efficiency.
2) For all operating regions, the voltage loss of power devices affects the slope of i_L and the distribution of positive power and negative power, and consequently influence the average power P_1 and P_2. Moreover, the voltage drop effect is more prominent for low-voltage applications than that for high voltage applications, where an external inductor is often used as the energy transfer element and high voltage will be applied to the inductor in latter case.

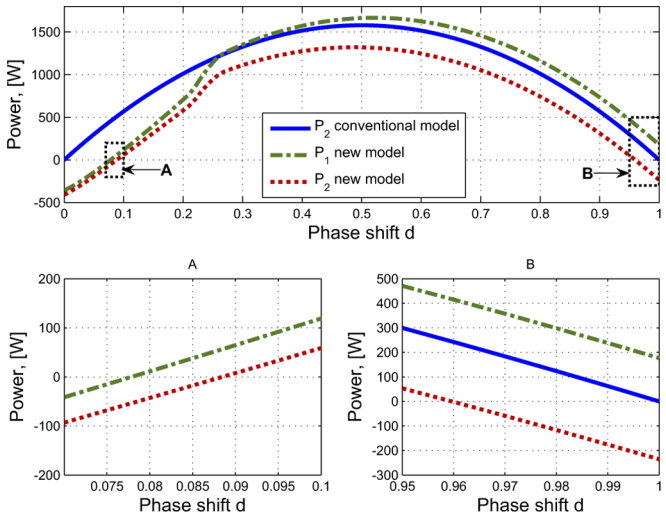


Fig. 12. Power flow characteristics for $V_1 = 30$ V, $V_2 = 80$ V, $V_s = 2$ V, $V_d = 1$ V, and $T_d = 2.5\,\mu$s.

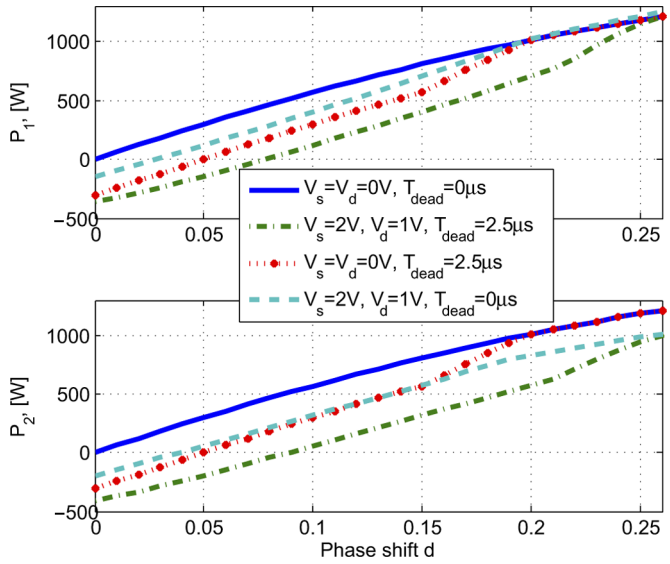


Fig. 13. Minor parameters impact on power flow characteristics for $V_1 = 30$ V and $d \in [0, 0.26]$.

Fig. 12 shows the power curves of the conventional model and the new model for $V_1 = 30$ V, $V_2 = 80$ V, $V_s = 2$ V, $V_d = 1$ V and $d \in [0, 1]$. If the minor parameters are nonzero, from the power flow curves calculated by the new model, if $0 \le d < 0.078$, then $P_1 < 0$ and $P_2 < 0$, indicating that the power flow direction is opposite to the desired direction (*reversed power flow*). For $0.078 \le d < 0.088$ or $0.96 \le d \le 1$, $P_1 > 0$ and $P_2 < 0$, the DAB converter acts as an energy sink (*energy sink*), meaning that the converter draws power from both the P_1 and P_2 ports and the energy is dissipated in the power devices. For $0.088 \le d \le 0.96$, we have $P_1 > 0$ and $P_2 > 0$, illustrating that the DAB converter delivers power with the desired direction. Moreover, at $d = 0.088$, the fact that $P_2 = 0$ suggests that the positive power and the negative power are canceled. So, the efficiency is extremely low (*Extremely Low Efficiency*) if the DAB converter operates at the region close to $d = 0.088$. Therefore, new characteristics such as *reversed power flow* and *energy sink* can be analytically identified and the *Extremely Low Efficiency* phenomenon also can be explained by the new power flow model. Moreover, the DAB converter reaches the maximum output power at $d = 0.5$. For the same output power, if the DAB converter operates in the $d < 0.5$ region, the input power is less than that of the converter operating in the $d > 0.5$ region, suggesting that the DAB converter should operate in the $d < 0.5$ region to achieve high efficiency. Actually, many DAB converters operates in a small d region [19], where the effect of the minor parameters is more significant, thus justifying the technical contribution of this paper. It is worthwhile to point out that both P_1 and P_2 calculated by the new model are equal to P_2 calculated by the conventional model for the whole operating range if the minor parameters V_s, V_d, and T_d are zero, suggesting that the new power flow model is consistent with the conventional analysis, as described in Section II.

Fig. 13 compares the effect of the minor parameters for $V_1 = 30$ V, $V_2 = 80$ V, $V_s = 2$ V, $V_d = 1$ V, and $0 \le d \le 0.26$ ($0 \le P_2 \le 1000$ W). It is obvious that the dead-time effect is more significant than the one of the voltage loss for P_1 model. For P_2 model, the dead-time effect is more prominent than the voltage loss for $d < 0.152$ while the voltage loss is more significant than the dead time for $0.152 \le d \le 0.26$. The voltage loss affects power flow for $d \in [0, 1]$, while the dead time only influences power flow for small phase shift d. Therefore, if we only consider the voltage loss, the power curves for both P_1 and P_2 converge to the curves with nonzero minor parameters. If we only consider the dead time, the power curves for both P_1 and P_2 converge to the curves with zero minor parameters.

To verify the effectiveness of the power flow model, experimental validation results will be presented in the next section.

V. Experimental Validation

A. Experimental Setup

Fig. 14(a) depicts the configuration of the experimental setup shown in Fig. 14(b). A DAB bidirectional dc/dc converter serves as an interface between the two dc buses whose voltages are regulated by a corresponding dc/dc converter. This setup enables investigation of power flow characteristics for the bidirectional dc/dc converter at different combinations of V_1 and V_2, over a wide operating range. The RT-LAB system[3] in Fig. 14(b) serves as the real-time control unit for the dc/dc converters and the data acquisition device. Parameters of the bidirectional dc/dc converter are shown in Table I.

B. Experimental Results

Fig. 15(a) shows the power curve of P_1 versus d, while Fig. 15(b) demonstrates the power curve of P_2 versus d for the DAB converter operating at $V_1 = 30$ V and $V_2 = 80$ V.

[3]RT-LAB is a distributed real-time platform that can perform real-time simulation, hardware in the loop test, and rapid control prototyping for large-scale system.

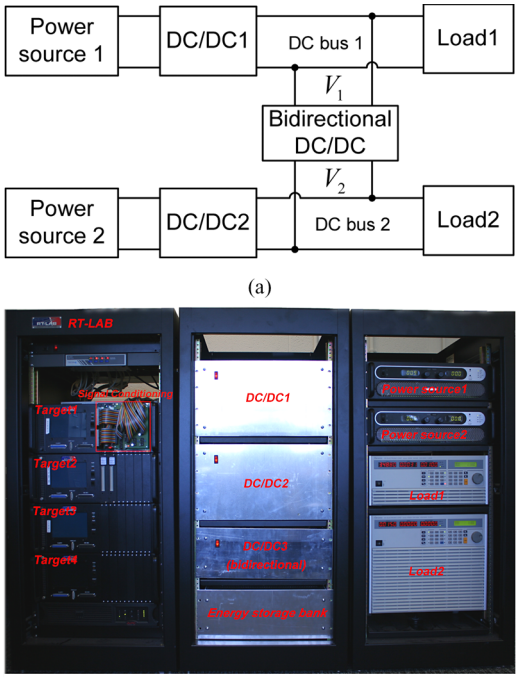


Fig. 14. Testbed of DAB converter. (a) Configuration. (b) Experiment setup.

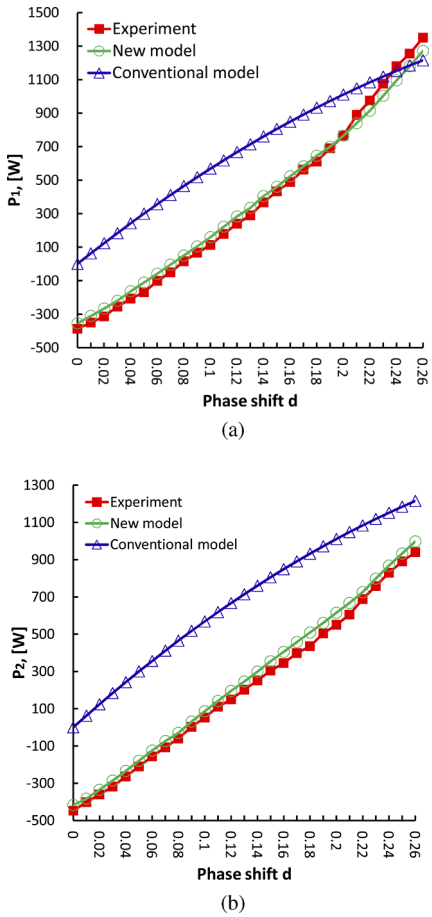


Fig. 15. Power flow curve for $V_1 = 30$ V. (a) P_1. (b) P_2.

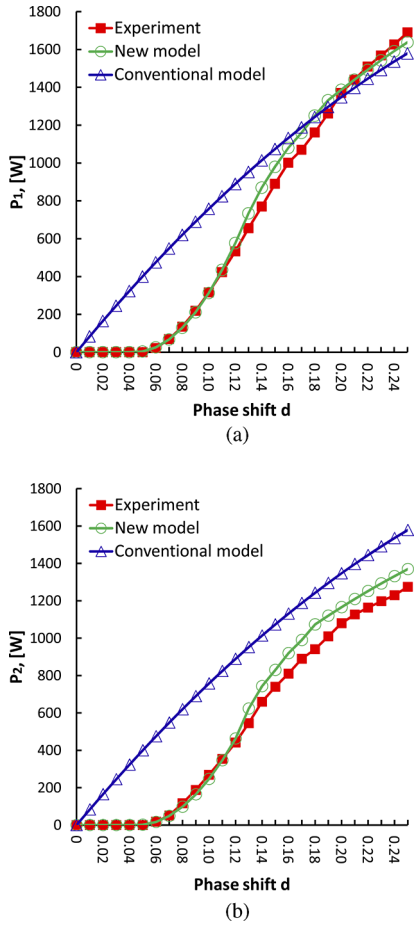
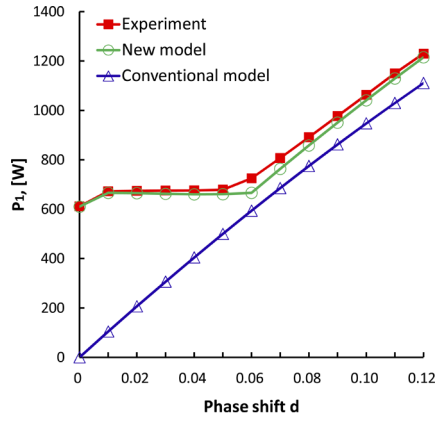


Fig. 16. Power flow curve for $V_1 = 40$ V. (a) P_1. (b) P_2.

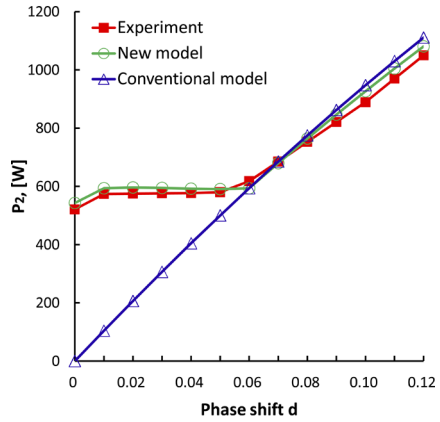
The experimental results validate the new power flow equation while the conventional power flow equation (characterized by the conventional model) shows significant error. Moreover, new characteristics *reversed power flow* and *energy sink* captured by the new power flow model are also explicitly confirmed.

Fig. 16 demonstrates the power curve of the DAB converter operating at $V_1 = 40$ V and $V_2 = 80$ V. For this case, the DAB converter works at region D for $0 \leq d \leq 0.05$ and region E for $0.05 \leq d \leq 0.12$, respectively. The new power flow model is much more accurate than the traditional power flow equation (characterized by the conventional model) because the minor parameters significantly affect the power flow of the DAB converter for these two regions. Note that there is no power transfer when $0 \leq d \leq 0.05$ (region D) for the reason as stated in Section IV. Once $d > 0.12$, the DAB converter operates at region F (no phase drift). At this region, P_2 calculated by the conventional model is larger than P_2 but smaller than P_1 given by the new model. Therefore, the conventional power flow equation is a good approximation in this region although the new model is still more accurate than the conventional one over a wide range of operating conditions.

Fig. 17 shows the power curve of the DAB converter operating at $V_1 = 50$ V and $V_2 = 80$ V. For this case, the DAB converter works at region G for $0 \leq d \leq 0.05$ and region H for $d > 0.05$,



(a)



(b)

Fig. 17. Power flow curve for $V_1 = 50$ V. (a) P_1. (b) P_2.

respectively. The new power flow model is much more accurate than the traditional power flow equation (characterized by the conventional model) in region G because of the significant impact of the minor parameters. In region H, the new model is still more accurate than the conventional one although the latter is also a good approximation at this region.

Together with the validation results for the internal power transfer phenomenon presented in Section III, we can draw the conclusion that the new power flow model is much more accurate than the conventional power flow model. The remaining difference between the new model predictions and the experiment results are likely due to unmodeled physical phenomena and modeled parameters uncertainties that could be a target of future investigation.

VI. Conclusion

This paper has presented a new power flow model for a DAB dc/dc converter over a wide operating range based on in-depth short-time-scale process analysis. In addition to those major parameters used by conventional power flow analysis, this new model incorporates minor parameters, namely the power semiconductor voltage loss and dead time. The minor parameters are critical for explaining the observed internal power transfer and phase drift phenomena, which are relevant to power flow characterization of the DAB converter. While the new model provides a more accurate prediction over a wide range of operating conditions, it also identifies new characteristics such as reverse power transfer and energy sink that are observed in experiments. Therefore, the new model can serve as a research tool for optimal hardware design, operating range selection, and power management strategy development. The experimental results illustrate the effectiveness of the new model.

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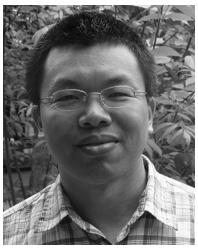

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