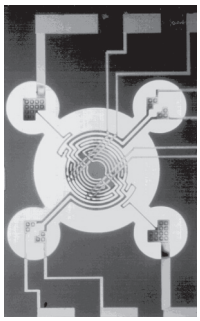
Steps in Microchip Fabrication



Chemical engineering principles are involved in virtually every step!

An abbreviated schematic of the steps involved in producing a typical metal-oxide, semiconductor, field-effect transistor (MOSFET) device is shown in Figure W10-1. Starting from the upper left, we see that single-crystal silicon ingots are grown in a Czochralski crystallizer, sliced into wafers, and chemically and physically polished. These polished wafers serve as starting materials for a variety of microelectronic devices. A typical fabrication sequence is shown for processing the wafer, beginning with the formation of an SiO_2 layer on top of the silicon. The SiO_2 layer may be formed either by oxidizing a silicon layer or by laying down a layer of SiO_2 by chemical vapor deposition (CVD). Next, the wafer is masked with a polymer photoresist, a template with the pattern to be etched onto the SiO_2 layer is placed over the photoresist, and the wafer is exposed to ultraviolet irradiation. If the mask is a positive photoresist, the light will cause the exposed areas of the polymer to dissolve when the

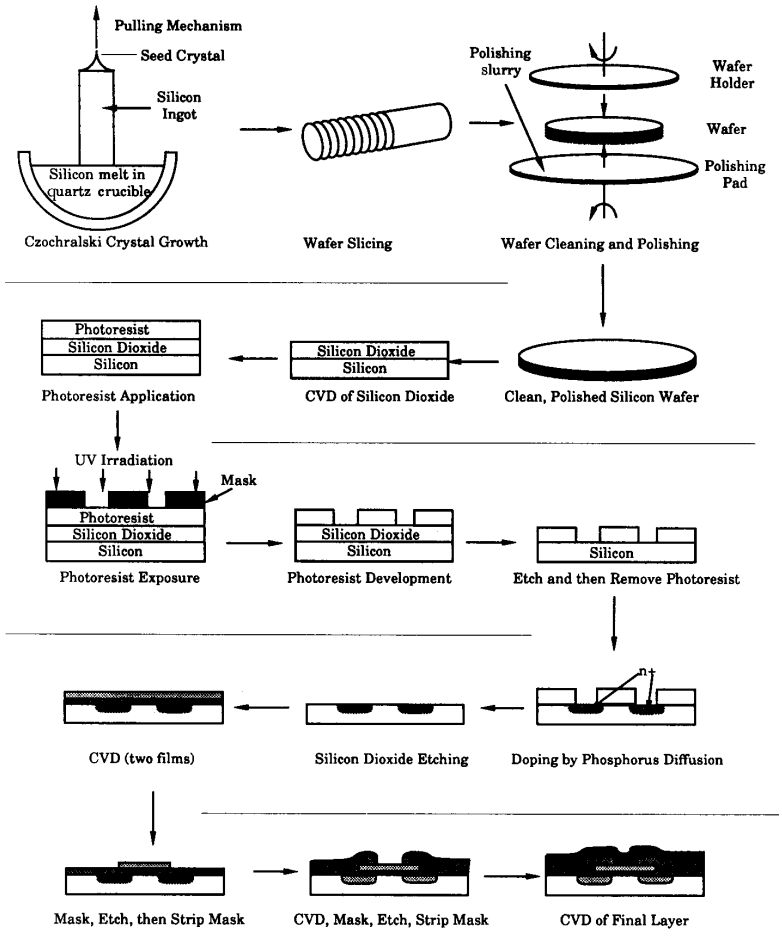


Figure W10-1 Microelectronic fabrication steps.

wafer is placed in the developer. On the other hand, when a negative photoresist mask is exposed to ultraviolet irradiation, cross-linking of the polymer chains occurs, and the *unexposed* areas dissolve in the developer. The undeveloped portion of the photoresist (in either case) will protect the covered areas from etching.

After the exposed areas of SiO_2 are etched to form trenches (either by wet etching or by plasma etching), the remaining photoresist is removed. Next, the wafer is placed in a furnace containing gas molecules of the desired dopant, which then diffuse into the exposed silicon. After diffusion of dopant to the desired depth in the wafer, the wafer is removed and then SiO_2 is removed by etching. The sequence of masking, etching, CVD, and metallization continues until the desired device is formed. A schematic of a final chip is shown in the lower right-hand corner of Figure W10-1. In Section 10.5.2, we discuss one of the key processing steps, CVD.